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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE


# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

Total Number of Pages in This Submission

| | |
|---|---|
| Application Number | 09/483,712 |
| Filing Date | January 14, 2000 |
| First Named Inventor | Jiang et al. |
| Art Unit | 2815 |
| Examiner Name | M. Warren |
| Attorney Docket Number | 2269-3815.1US (98-0670.00/US) |

**ENCLOSURES** ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
  - Claims Appendix
  - Evidence Appendix
  - Related Proceeding Appendix

**Remarks**

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

| | | | |
|---|---|---|---|
| Firm | TraskBritt, P.C. | | |
| Signature | | | |
| Printed Name | J. Jeffrey Gunn | | |
| Date | March 7, 2007 | Reg. No. | 56,957 |

**CERTIFICATE OF MAILING**

Express Mail Label Number: EV826304010US

Date of Deposit: March 7, 2007

Person Making Deposit: Cat Bratton

PTO/SB/17 (12-04v2)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE


*Effective on 12/08/2004.*
*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*



# FEE TRANSMITTAL for FY 2007

☐ Applicant claims small entity status. See 37 CFR 1.27

| TOTAL AMOUNT OF PAYMENT | ($) 500.00 |
|---|---|

| Complete if Known | |
|---|---|
| Application Number | 09/483,712 |
| Filing Date | 1/14/2000 |
| First Named Inventor | Jiang et al. |
| Examiner Name | M. Warren |
| Art Unit | 2815 |
| Attorney Docket No. | 2269-3815.1US (98-0670.00/US) |

## METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify) : _____

☒ Deposit Account Deposit Account Number: 20-1469 Deposit Account Name: TraskBritt, PC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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## FEE CALCULATION

### 1. BASIC FILING, SEARCH, AND EXAMINATION FEES

| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
|---|---|---|---|---|---|---|---|
| | | Small Entity | | Small Entity | | Small Entity | |
| Application Type | Fee ($) | Fee($) | Fee($) | Fee($) | Fee($) | Fee($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | ____ |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | ____ |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | ____ |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | ____ |
| Provisional | 200 | 100 | 0 | 0 | 0 | 0 | ____ |

### 2. EXCESS CLAIM FEES

| Fee Description | Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 (including Reissues) | 50 | 25 |
| Each independent claim over 3 (including Reissues) | 200 | 100 |
| Multiple dependent claims | 360 | 180 |

| Total Claims | | Extra Claims | | Fee($) | | Fee Paid ($) |
|---|---|---|---|---|---|---|
| ____ | -20 or HP= | ____ | x | ____ | = | ____ |

HP = highest number of total claims paid for, if greater than 20.

| Indep. Claims | | Extra Claims | | Fee($) | | Fee Paid ($) |
|---|---|---|---|---|---|---|
| ____ | - 3 or HP= | ____ | x | ____ | = | ____ |

HP = highest number of independent claims paid for, if greater than 3.

| Multiple Dependent Claims | |
|---|---|
| Fee ($) | Fee Paid ($) |
| ____ | ____ |

### 3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | | Extra Sheets | | Number of each additional 50 or fraction thereof | | Fee ($) | | Fee Paid ($) |
|---|---|---|---|---|---|---|---|---|
| ____ | - 100 = | ____ | / 50 = | ____ | (round up to a whole number) x | | = | ____ |

### 4. OTHER FEE(S)

| | Fees Paid ($) |
|---|---|
| Non-English Specification, $130 fee (no small entity discount) | ____ |
| Other (e.g., late filing surcharge) : Filing a Brief in Support of an Appeal | 500.00 |

## SUBMITTED BY

| | | | |
|---|---|---|---|
| Signature | | Registration No. (Attorney/Agent) 56,957 | Telephone 801-532-1922 |
| Name (Print/Type) | J. Jeffrey Gunn | Date | March 7, 2007 |

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**In re Application of:**

Jiang et al.

**Serial No.:** 09/483,712

**Filed:** January 14, 2000

**For:** INTERMEDIATE STRUCTURES FOR CHIP-SCALE PACKAGES HAVING CARRIER BONDS (as amended)

**Confirmation No.:** 8743

**Examiner:** M. Warren

**Group Art Unit:** 2815

**Attorney Docket No.:** 2269-3815.1US
(98-0670.00/US)

NOTICE OF EXPRESS MAILING

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Date of Deposit with USPS: March 7, 2007

Person making Deposit: Cat Bratton

## APPEAL BRIEF

Mail Stop Appeal Brief – Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sirs:

This brief is submitted in the format required under 37 C.F.R. § 41.37(c). A check in the amount of $500.00 for the fee under 37 C.F.R. § 41.20(b)(2) for filing a brief in support of an appeal is enclosed.

1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., Assignee of the pending application as recorded with the United States Patent and Trademark Office on January 14, 2000, at Reel 010532, Frame 0640.

2) RELATED APPEALS AND INTERFERENCES

The Appellants, the Appellants' representative, and the Assignee are not aware of any pending appeal or interference that would relate to, directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

3) STATUS OF THE CLAIMS

Claims 1 through 16 and 19 are pending in the application.

Claims 17, 18, and 20 through 29 are canceled.

Claims 1 through 16 and 19 stand rejected.

No claims are allowed.

Claims 1 through 16 and 19 are the subject of the pending appeal.

4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed September 6, 2006.

5) SUMMARY OF THE CLAIMED SUBJECT MATTER

The presently claimed invention is directed to intermediate structures formed during fabrication of so-called "chip-scale packages," such as the embodiments of the chip-scale package 100 shown in Figures 2 through 6 of the as-filed application for the present invention (hereinafter "the Application"), which are a type of semiconductor device. In particular, the claimed invention in the present application is an intermediate structure formed during fabrication of a chip-scale package that includes a semiconductor die 10 having at least one bond pad 12 on an active surface 11 of the semiconductor die 10. The Application, Page 6, Lines 14-26; Figures 2-5. At least one discrete conductive bond 16, 40 connects an end of a conductive lead frame member 14, 20 to the at least one bond pad 12. Id. at Page 6, Lines 14-15; page 8, lines 7-15; Figures 2-5. At least one carrier bond 18, 50 is attached to an upper surface of the conductive lead frame member 14, 20 and extends transversely thereto. Id. at Page 6, Line 26 – Page 7, Line 2; Page 7, Lines 19-21; Page 8, Lines 16-24; Figures 2-5. Also, the intermediate structure is free of encapsulant material 60 that is to be subsequently applied to the intermediate structure to form the chip-scale package 100. Id., Page 9, Lines 4-14; Page 10, Lines 15-21. In some embodiments, the carrier bonds 18, 50 comprise a conductive or conductor-filled epoxy material. The Application, Page 5, Lines 6-8; Page 8, Lines 19-23; Claim 14.

6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The First Rejection

Appellants request that the Board review the rejection of Claims 1, 2, 5 through 9, 13 through 16, and 19 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 5,677,566 to King et al. (hereinafter "King et al.") in view of United States Patent Application Publication No. 2001/0011773 A1, filed by Havens et al (hereinafter "Havens et al."), which was made in a Final Office Action mailed September 6, 2006 (hereinafter "the Final Action").

(B) The Second Rejection

Appellants additionally request that the Board review the rejection of Claims 3, 4, and 10 through 12 under 35 U.S.C. § 103(a) as being unpatentable over King et al. and Havens et al. in further view of United States Patent No. 5,894,107 to Lee et al. (hereinafter "Lee et al."), which also was made in the Final Office Action.

7) ARGUMENT

(A) The First Rejection

(i) Claims 1, 2, 5-9, 13, 15, 16, and 19

Appellants assert that the U.S. Patent and Trademark Office (the "Office") has failed to establish a *prima facie* case of obviousness with respect to Claims 1, 2, 5 through 9, 13, 15, 16, and 19 because the Office has failed to identify a sufficient motivation to combine the teachings of King et al. with the teachings of Havens et al. in the manner proposed by the Office.

Rejection of claims under 35 U.S.C. § 103(a) requires that the Office establish a *prima facie* case of obviousness. M.P.E.P. § 2142. M.P.E.P. 706.02(j) sets forth the standard for an obviousness rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. **First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings.** Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

To provide a motivation or suggestion to combine, the prior art or the knowledge of a person of ordinary skill in the art must "suggest the desirability of the combination" or provide "an objective reason to combine the teachings of the references." M.P.E.P. § 2143.01. It is improper to combine references where the references teach away from combination. M.P.E.P. § 2145.

Appellants admit that King et al. teaches a final chip-scale package substantially similar to the final chip-scale package taught in the application for the present invention. Appellants and the Office appear to agree, however, that King et al. teaches (with respect to Figures 4 through 8 therein) a method of manufacturing the chip-scale package in which the carrier bonds are attached to the conductive leads after encapsulation, but does not teach or suggest a method in which the carrier bonds are attached to the conductive leads prior to encapsulation, as taught at Page 9, lines 4 through 14 of the Application for the present invention. As such, Appellants and the Office further appear to agree that King et al. does not teach or suggest an intermediate

structure as claimed in either of independent Claims 1 and 2, in which at least one carrier bond is directly attached to (Claim 1) or disposed on (Claim 2) the upper surface of at least one conductive lead frame member of the intermediate structure, and the intermediate structure is free of an encapsulant material.

The Office has asserted that although King et al. does not teach such as intermediate structure, one of ordinary skill in the art, considering King et al. in view of Havens et al., would have been motivated to combine the teachings of Havens et al. with the teachings of King et al. in such a way as to provide an intermediate structure as recited in each of independent Claims 1 and 2. Appellants respectfully disagree for the reasons set forth below.

Havens et al. teaches a hydrophobic hermetic covering that can be applied to substantially all external surfaces of an electronic package, and methods of applying the hydrophobic hermetic covering to external surfaces of an electronic package. Havens et al., Page 2, Paragraph [0025]. Havens et al. teaches that the hermetic covering may comprise a thin layer (e.g., 0.001 inches) of Teflon® material or another fluorinated thermoset material. Id., Page 3, Paragraphs [0031], [0033], [0037].

Havens et al. teaches that carrier bonds (e.g., solder balls 6) can be applied to a substrate 3 of an electronic package 1 before applying the hydrophobic hermetic covering to the package 1 (Havens et al., Page 2, Paragraph [0028] – Page 3, Paragraph [0031]), or after applying the hydrophobic hermetic covering to the package 1 (Id., Page 5, Paragraphs [0057]-[0058]).

Appellants admit that one of ordinary skill in the art, considering the combined teachings of King et al. and Havens et al. as a whole at the time the present invention was made, may have

been motivated to replace the encapsulating material 26 of the device taught by King et al. (See e.g., King et al., column 3, lines 28-33) with a hermetic covering as taught in Havens et al. to address the moisture sensitivity problem addressed by Havens et al. (See e.g., Havens et al., Page 1, Paragraphs [0002]-[0003]; Page 2, Paragraph [0025]). Appellants respectfully assert, however, that in so doing, one of ordinary skill in the art would have been motivated to attach the carrier bonds to the conductive leads of the device taught by King et al. *after* applying the hermetic covering, and *not before*, as asserted by the Office.

As previously mentioned, King et al. teaches attaching the carrier bonds (external electrodes 28) after applying the encapsulating material. King et al., Column 4, Lines 35-65. Havens et al. also teaches that the carrier bonds (solder balls 6) may be attached after applying the hermetic covering to the package. As a result, this method is in accordance with both the teachings of King et al. and Havens et al., and as such, clearly would have been the obvious method of choice to one of ordinary skill in the art at the time the present invention was made. While Havens et al. teaches that the carrier bonds 6 may be attached to the electronic package 1 either before or after applying the hermetic covering, there is no reason one of ordinary skill in the art would be motivated to further and unnecessarily modify the teachings of King et al. so as to attach the carrier bonds before applying the hermetic covering. In other words, the prior art references do not teach or suggest the desirability of attaching the carrier bonds before applying the hermetic covering as opposed to attaching the carrier bonds after applying the hermetic covering.

The Office appears to assert at Pages 6-7 of the outstanding Office Action that Havens et al. teaches that attaching the carrier bonds to the conductive leads of the device taught therein before applying the hermetic covering would improve reliability and product yield, and hence, one of ordinary skill in the art would have been motivated at the time the present invention was made to attach the carrier bonds to the conductive leads of the device taught therein after applying the hermetic covering of Havens et al. to the structure of King et al. to improve reliability and product yield. Appellants note, however, that Havens et al. teaches that the invention taught therein "largely solves the moisture sensitivity problem associated with electronic packages by covering substantially all of the external surfaces of the electronic package, *with the exception of a portion of the conductors that are required for electrically coupling to an external substrate*, with an essentially hermetic covering which is highly hydrophobic," and that "the reduced level of moisture improves product yields and reliability thru the final assembly and testing processes." Havens et al., Page 2, Paragraph [0025] (emphasis added). Whether the carrier bonds are attached to the conductive leads of the device before or after applying the hermetic covering, substantially all of the external surfaces of the electronic package are covered by the hermetic covering, with the exception of a portion of the conductors that are required for electrically coupling to an external substrate. Therefore, Havens et al. clearly teaches that the hermetic covering improves reliability and product yield regardless of whether the carrier bonds are attached before or after applying the hermetic covering.

The Office also notes at Pages 6-7 of the outstanding Office Action that Havens et al. states "[i]n one embodiment, all of the package, including all of the external conductor surfaces,

are covered (e.g., to facilitate shipment)," and appears to assert that this statement teaches or suggests that attaching the carrier bonds to the conductive leads of the device taught therein before applying the hermetic covering of Havens et al. to the structure of King et al. would "facilitate shipment" of the resulting structure. Appellants respectfully disagree. Havens et al. provides no indication whatsoever as to how shipment is facilitated by covering all external surfaces of the package with the hermetic covering. There is simply no description, teaching, or suggestion in Havens et al. as to how shipment of a package in which all of the external conductor surfaces are covered with the hermetic covering is improved, enhanced, or otherwise facilitated relative to shipment of a package in which substantially all of the external surfaces of the electronic package are covered with the hermetic covering, with the exception of a portion of the conductors that are required for electrically coupling to an external substrate, as in embodiments in which the carrier bonds are attached after applying the hermetic covering. In fact, Havens et al. expressly teaches that an electronic package having a "hydrophobic protective covering over substantially all of the external surfaces of the package, except for those portions of conductors that were covered by the cover layer," is "ready for shipment." Havens et al., Page 4, Paragraph [0047].

Furthermore, Appellants respectfully assert that one of ordinary skill in the art would recognize that, in methods in which the carrier bonds are attached after applying the hermetic covering, the electronic package could be shipped prior to attaching the carrier bonds, in which case all of the package, including all of the external surfaces, would be covered by the hermetic covering.

In sum, there simply is no teaching or suggestion in the cited prior art references that any benefit would be achieved by attaching the carrier bonds to the conductive leads of the device taught by King et al. prior to applying the hermetic covering taught by Havens et al. In other words, the prior art references do not teach or suggest the desirability of attaching the carrier bonds to the conductive leads in the device taught by King et al. before applying the hermetic covering of Havens et al. instead of after applying the hermetic covering. In contrast, however, attaching the carrier bonds to the conductive leads of the device taught by King et al. after applying the hermetic covering taught by Havens et al. accords with the teachings of both Havens et al. and King et al. and would require less modification of the teachings of King et al. Therefore, one of ordinary skill in the art, considering the teachings of King et al. and Havens et al. in combination and as a whole at the time the present invention was made, clearly would have been motivated to attach the carrier bonds to the leads of the device after applying the hermetic covering taught by Havens et al. to the device taught by King et al.

Appellants respectfully assert that the Office appears to be using improper hindsight and combining the cited prior art references solely on the basis of the Appellants disclosure in the present application.

As there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, Appellants respectfully assert that the Office has failed to establish a *prima facie* case of obviousness with

respect to each of independent Claims 1 and 2, and request that the Board overturn the rejection of independent Claims 1 and 2 under 35 U.S.C. § 103(a).

Furthermore, Appellants assert that the non-obviousness of independent Claim 2 precludes a rejection of Claims 5 through 9, 13, 15, 16, and 19, each of which depends from Claim 2, because a dependent claim is obvious only if the independent claim from which it depends is obvious. See, In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), see also MPEP § 2143.03. At least for this reason, Appellants request that the Board overturn the rejection of dependent Claims 5 through 9, 13, 15, 16, and 19 under 35 U.S.C. § 103(a).

(ii) Claim 14

Appellants submit that the obviousness rejection of Claim 14 is improper and should be reversed because the Office has failed to identify a sufficient motivation to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, as previously discussed in Section (7)(A)(i) above.

Appellants also assert that the obviousness rejection of Claim 14 is improper and should be reversed for the additional reason that King et al. and Havens et al., when combined, do not teach or suggest all the limitations of Claim 14. In particular, Appellants assert that King et al. and Havens et al., when combined, do not teach or suggest "[a] plurality of conductive carrier bonds [comprising] a conductive or conductor-filled polymer," as recited in dependent Claim 14.

King et al. teaches that the external electrodes 28 (shown in Figures 1 through 5 and 8 thereof) may comprise solder balls (King et al., Column 2, Lines 23-26; Column 4, Lines 49-65),

but does not teach or suggest that they may comprise a conductive or conductor-filled polymer. Similarly, Havens et al. teaches that the conductors 6 (shown in Figures 1, 1A, 1B, 2, 2A, 3, 3A, 4, 4A, 5, 6, 6A, and 7) thereof may comprise solder balls ( Havens et al., Page 2, Paragraph [0028]; Page 3, Paragraph [0030]; Page 4, Paragraph [0046]; Page 5, Paragraphs [0056]-[0058]), but does not teach or suggest that they may comprise a conductive or conductor-filled polymer.

As there is no suggestion or motivation to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, and because King et al. and Havens et al. do not teach or suggest all the limitations of Claim 14, Appellants respectfully assert that the Office has failed to establish a *prima facie* case of obviousness with respect to dependent Claim 14, and request that the Board overturn the rejection of dependent Claim 14 under 35 U.S.C. § 103(a).

(B) The Second Rejection

(i) Claims 3, 4, and 10-12

Each of Claims 3, 4, and 10 through 12 depends either directly or indirectly from independent Claim 2, and, as a result, each includes the limitations recited in independent Claim 2. Appellants assert that the U.S. Patent and Trademark Office (the "Office") has failed to establish a *prima facie* case of obviousness with respect to Claims 3, 4, and 10 through 12 because the Office has failed to identify a sufficient motivation to combine the teachings of King et al. with the teachings of Havens et al. in the manner proposed by the Office.

As previously discussed in Section (7)(A)(i), King et al. and Havens et al., when combined, do not teach or suggest an intermediate structure as recited in independent Claim 2, from which each of Claims 3, 4, and 10 through 12 depends. The teachings of Lee et al. do not satisfy the deficiencies.

Lee et al. teaches providing a plurality of carrier bonds in the form of solder balls 16 on exposed upper surfaces of external connection means 34 *after* encapsulating a chip and lead frame assembly. Lee et al., Column 5, Lines 20-29, and 39-43; Figures 11-12. Therefore, Lee et al. also fails to provide any teaching or suggestion for forming external electrodes 28 on the conductive leads 12 of King et al. before providing a hermetic covering as taught by Havens et al. thereon in such a manner as to provide an intermediate structure as recited in independent Claim 2.

As there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, Appellants respectfully assert that the Office has failed to establish a *prima facie* case of obviousness with respect to each of dependent Claims 3, 4, and 10 through 12, and request that the Board overturn the rejection of these Claims under 35 U.S.C. § 103(a).

8) CLAIMS APPENDIX

A copy of Claims 1 though 16 and 19, as currently pending, is appended hereto in a "Claims Appendix."

9) EVIDENCE APPENDIX

The following documents are appended hereto as exhibits in an "Evidence Appendix:"

A copy of United States Patent No. 5,677,566 (King et al.) is appended hereto as "Evidence Exhibit 1."

A copy of United States Patent Application Publication No. 2001/0011773 A1 (Havens et al.) is appended hereto as "Evidence Exhibit 2."

A copy of United States Patent No. 5,894,107 (Lee et al.) is appended hereto as "Evidence Exhibit 3."

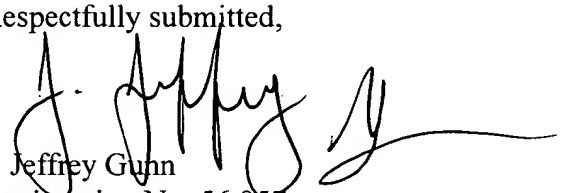
10) RELATED PROCEEDINGS APPENDIX

None

## CONCLUSION

Appellants respectfully submit that Claims 1 through 16 and 19 are allowable over the cited references of record. Appellants respectfully request that the rejections of Claims 1 through 16 and 19 under 35 U.S.C. § 103(a) be reversed.

Respectfully submitted,



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Date: March 7, 2007
JJG/dlm:slm

Document in ProLaw

# CLAIMS APPENDIX

**U.S. Patent Application No. 09/483,712**

**Filed January 14, 2000**

**Claims 1-16 and 19**

1. An intermediate structure in the fabrication of a chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon, sides and a back side;

at least one conductive lead frame member laterally spaced from the at least one bond pad and having an upper surface and a lower surface, the lower surface of the at least one conductive lead frame member having and inner end and an outer end and being substantially non-conductively attached to a portion of the active surface of the semiconductor die and vertically spaced therefrom by a non-coextensive dielectric element interposed therebetween;

at least one discrete conductive bond connecting the inner end of the at least one conductive lead frame member to the at least one bond pad on the active surface of the semiconductor die;

at least one carrier bond directly attached to the upper surface of the at least one conductive lead frame member at the outer end thereof and extending transversely thereto; and

wherein the intermediate structure is free of an encapsulant material to be subsequently applied to the intermediate structure.

2. An intermediate structure in the fabrication of a chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;

a dielectric element having an upper surface and a lower surface, the lower surface of the dielectric element attached to a portion of the active surface of the semiconductor die;

a plurality of conductive lead frame members having inner ends laterally spaced from the plurality of bond pads, each conductive lead frame member of the plurality of conductive lead frame members having an upper surface and a lower surface, a portion of the lower surface of each conductive lead frame member of the plurality of conductive lead frame members being attached to a portion of the upper surface of the dielectric element for connecting each conductive lead frame member of the plurality of conductive lead frame members to the active surface of the semiconductor die;

a plurality of discrete conductive bond members, at least one discrete conductive bond member of the plurality of conductive bond members connecting the inner end of each conductive lead frame member of the plurality of conductive lead frame members to at least one bond pad of the plurality of bond pads on the active surface of the semiconductor die;

a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds directly disposed on the upper surface of each conductive lead frame member of the plurality of conductive lead frame members at a location remote from the inner end thereof and extending transversely from the upper surface thereof; and

wherein the intermediate structure is free of an encapsulant material to be subsequently applied to the intermediate structure.

3. An intermediate structure as in claim 2, wherein the dielectric element includes an adhesive-coated polyimide tape.

4. An intermediate structure as in claim 2, wherein the dielectric element includes a polyimide film.

5. An intermediate structure as in claim 2, wherein the upper surface and lower surface of the dielectric element are attached respectively to a portion of the lower surface of each conductive lead frame member of the plurality of conductive lead frame members and a portion of the active surface of the semiconductor die connecting portions of the plurality of conductive lead frame members to portions of the active surface of the semiconductor die.

6. An intermediate structure as in claim 2, wherein the plurality of conductive lead frame members comprises a plurality of lead fingers.

7. An intermediate structure as in claim 2, wherein the plurality of conductive lead frame members comprises a conductive metal.

8. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises a conductive metal.

9. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises bond wires.

10. An intermediate structure as in claim 9, wherein the bond wires comprise gold or aluminum.

11. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises TAB bonds.

12. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises thermocompression bonds.

13. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds includes metal.

14. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds is selectively located on the upper surfaces of the plurality of conductive lead frame members, forming an array over the active surface of the semiconductor die.

16. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds comprises solder balls.

19. An intermediate structure as in claim 2, wherein each conductive carrier bond of the plurality of conductive carrier bonds further comprises an upper portion and a lower portion, the lower portion of each conductive carrier bond being attached to the upper surface of an associated conductive lead frame member of the plurality of conductive lead frame members.

# EVIDENCE APPENDIX

**U.S. Patent Application No. 09/483,712**

**Filed January 14, 2000**

**Evidence Exhibit 1 - United States Patent No. 5,677,566**

**Evidence Exhibit 2 - United States Patent Application Publication No. 2001/0011773 A1**

**Evidence Exhibit 3 - United States Patent No. 5,894,107**